

WHAT IS CLAIMED IS:

1. A numeric counter oscillator comprising:

a quotient accumulator, the quotient accumulator having a programmable input for receiving a QUOTIENT value, a reference clock input and a multi-bit output, the output adapted for transmitting an output value OUT representing an accumulated quotient sum, the multi-bit output incrementing by a predetermined amount in response to each reference clock period;

a remainder accumulator, the remainder accumulator having programmable inputs for receiving respective REMAINDER and DIVISOR values, a reference clock input and a multi-bit output representing an accumulated digital remainder sum less than a predefined digital integer, the remainder accumulator further comprising a comparator having a first input for receiving a programmed divisor value, and a second input for receiving the remainder accumulator multi-bit output, the comparator operative to generate an increment carry signal for application to the quotient accumulator when the remainder multi-bit output reaches the predefined integer value.

2. A numeric counter oscillator according to claim 1 wherein the quotient accumulator comprises:

a shift register having a clock input for receiving the input reference clock signal;

a first summing stage for receiving the quotient input, and comprising a second input coupled to the accumulator output; and

a second summing stage disposed in series with the first stage and having an input coupled to the comparator output to receive the carry increment signal, the second summing stage further comprising an output coupled to the input of the shift register.

3. A numeric counter oscillator according to claim 1 wherein the remainder accumulator comprises:

a third summing stage having an input for receiving the REMAINDER value;

5 a subtractor with a pair of inputs for receiving, respectively, the summed output from the third summing stage and the DIVISOR value; and

a second shift register for incrementing the remainder accumulator output in response to the input clock, and feeding back the output to the third summing stage.

10 4. A numeric counter oscillator for providing a numerical solution to the relationship A/B , where B comprises a DIVISOR, and the decimal solution comprises a QUOTIENT + REMAINDER, the numerical counter oscillator comprising:

5 means for accumulating a quotient sum in response to an input QUOTIENT value; and

means for generating a remainder sum in response to a REMAINDER input value and a DIVISOR input value, the means for generating a remainder sum comprising means for generating a carry signal to increment the quotient sum when the remainder sum equates to the DIVISOR input value.

10 5. A numeric counter oscillator according to claim 4 wherein the means for accumulating a quotient sum comprises:

a quotient accumulator, the quotient accumulator having a programmable input for receiving a QUOTIENT value, a reference clock input and a multi-bit output, the output adapted for transmitting an output value OUT representing an accumulated quotient sum, the multi-bit output incrementing by a predetermined amount in response to each reference clock period.

25 6. A numeric counter oscillator according to claim 4 wherein the means
for accumulating a remainder sum comprises:

 a remainder accumulator, the remainder accumulator having
programmable inputs for receiving respective REMAINDER and DIVISOR values, a
a reference clock input and a multi-bit output representing an accumulated digital
30 remainder sum less than a predefined digital integer, the remainder accumulator
further comprising a comparator having a first input for receiving a programmed
divisor value, and a second input for receiving the remainder accumulator multi-bit
output, the comparator operative to generate an increment carry signal for application
to the quotient accumulator when the remainder multi-bit output reaches the
35 predefined integer value.

 7. A method of generating a desired numeric counter oscillator frequency
based on a reference frequency, the desired frequency and reference frequency having
the relationship A/B , where B comprises a DIVISOR, and the decimal solution
comprises a QUOTIENT + REMAINDER, the method including the steps:
5 generating a reference clock having the reference frequency and period;
 incrementing a first accumulator for each reference waveform period,
the first accumulator having a QUOTIENT input and an output for keeping track of an
accumulated sum;
 incrementing a second counter by each reference waveform period, the
10 second counter having a divisor input DIVISOR related to the QUOTIENT input for
keeping track of a remainder sum; and
 comparing the remainder sum to the DIVISOR input, and when the
remainder sum reaches the DIVISOR value, generating a carry increment for
accumulation in the first counter.

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